connection terminal,

wherein said electrically insulating layer serves to relax a stress produced between said semiconductor apparatus and a substrate on which said semiconductor apparatus is mounted, and

wherein said wiring includes a copper layer and a nickel layer formed on said copper layer.

~~24.~~ A semiconductor apparatus according to claim 23, wherein each of said copper layer and said nickel layer is formed by electroplating.

~~25.~~ A semiconductor apparatus according to claim 23, wherein said wiring is in a two-layered structure having said copper and nickel layers, each of said copper layer and said nickel layer being formed by electroplating, and said nickel layer covers said copper layer.

~~26.~~ A semiconductor apparatus according to claim 23, wherein, when said copper layer is deformed subject to deformation of said electrically insulating layer, said nickel layer serves to restore said copper layer to its original shape before deformation.

~~27.~~ A semiconductor apparatus according to claim 23, wherein said wiring has one end serving also as a bump pad.

~~28.~~ A semiconductor apparatus according to claim 23, wherein said electrically insulating layer is formed by printing by use of a mask.

29. A semiconductor apparatus according to claim 23, wherein said electrically insulating layer contains particles. 6376100 Cc, 23-28

30. A semiconductor apparatus according to claim 23, wherein said electrically insulating layer has an inclination portion, and, wherein a power/ground line in said wiring on said inclination portion of said electrically insulating layer has a shape different from that of a signal line in said wiring on said inclination portion of said electrically insulating layer.

31. A semiconductor apparatus according to claim 30, wherein said power/ground line on said inclination portion of said electrically insulating layer has a width larger than that of said signal line in said wiring on said inclination portion of said electrically insulating layer.

Cancel.

32. A semiconductor apparatus according to claim 23, wherein said wiring has its width increased on an edge portion of said electrically insulating layer.

33. A semiconductor apparatus according to claim 23, wherein said external connection terminal has a first external connection terminal member formed on a flat portion of said electrically insulating layer having a substantially constant thickness and a second external connection terminal member formed on an inclination portion of said electrically insulating layer.